

ABSTRACT

A signal routing apparatus comprises a register bank to store a set of data signals. A delay locked loop generates a set of phase displaced clock signals. A phase controlled read circuit sequentially routes the set of data signals from the register bank
5 in response to the phase displaced clock signals. A Low Voltage Differential Signaling buffer connected to the phase controlled read circuit transmits the data signals in a Low Voltage Differential Signaling mode. The phase displaced clock signals operate in lieu of a higher clock rate in order to reduce power consumption.

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